AMENDMENT TO THE CLAIMS

The following listing of claims replaces all prior versions and listings in the application.

Listing of Claims:

1. (Currently Amended) A method of compiling a circuit interconnect model, comprising:

providing extraction data from [[an]] a circuit interconnect;

reading a dataset from said extraction data from said circuit interconnect;

~~reducing~~ translating said dataset to form a model of said circuit interconnect including parasitic electrical properties;

evaluating said model for a set of conditions to obtain a ~~solution~~ measure of performance of said circuit interconnect under the influence of said parasitic electrical properties; and

writing said measure of performance ~~solution~~ to an application.

2. (Currently Amended) The method of claim 1, further comprising, after ~~reducing~~ translating said dataset to form a model, writing said model to a parasitic database and, before evaluating said model, reading said model from said parasitic database.

3. (Currently Amended) The method of claim [[2]] 1, wherein ~~writing~~ translating said dataset to ~~said parasitic database~~ form a model includes using a view translator plug-in.

4. (Original) The method of claim 1, further comprising providing a circuit database and writing a name map.

5. (Original) An electronic media, comprising a program for performing the method of claim 1.

6. (Original) A computer program, comprising computer or machine readable program elements translatable for implementing the method of claim 1.

7. (Original) An integrated circuit designed in accordance with the method of claim 1.

8. (Original) The method of claim 1, further comprising verifying a design of an integrated circuit.

9. (Original) A computer program comprising computer program means adapted to perform the steps of

providing extraction data from [[an]] a circuit interconnect;

reading a dataset from said extraction data from said circuit interconnect;

~~reducing~~ translating said dataset to form a model of said circuit interconnect including parasitic electrical properties;

evaluating said model for a set of conditions to obtain a ~~solution~~ measure of performance of said circuit interconnect under the influence of said parasitic electrical properties; and

writing said measure of performance ~~solution~~ to an application.

10. (Original) A computer program as claimed in claim 9, embodied on a computer-readable medium.

AMENDMENT TO THE SPECIFICATION

Please replace the paragraph spanning pages 2 and 3 with the following amended paragraph:

One embodiment of the invention is based on a method of compiling a circuit interconnect model, comprising: providing extraction data from an interconnect; reading a dataset from said extraction data from said interconnect; ~~reducing~~ translating said dataset to form a model; evaluating said model for a set of conditions to obtain a solution; and writing said solution to an application. Another embodiment of the invention is based on an electronic media, comprising a program for performing this method. Another embodiment of the invention is based on a computer program, comprising computer or machine readable program elements translatable for implementing this method. Another embodiment of the invention is based on an integrated circuit designed in accordance with this method. Yet another embodiment of the invention is based on a computer program comprising computer program means adapted to perform the steps of providing extraction data from an interconnect; reading a dataset from said extraction data from said interconnect; ~~reducing~~ translating said dataset to form a model; evaluating said model for a set of conditions to obtain a solution; and writing said solution when said program is run on a computer.

Please replace the second full paragraph on page 9 with the following amended paragraph:

A set of parasitic/extraction data 610 from an interconnect of interest may be used by an interconnect model compiler 620. The set of parasitic/extraction data 610 can contain information on the electrical properties of some/many/all of the interconnects in the design of interest. The interconnect model compiler 620 may include a compiler socket 625. The compiler socket 625 includes a location a plug-in engages. The compiler socket [[765]] 625 can be adapted to receive/support one, or more, plug-in(s) 630.

Please replace the third full paragraph on page 9 with the following amended paragraph:

The system 600 can also include a cell library .LIB 635. The cell library .LIB 635 can be coupled to an open model compiler 645. The open model compiler 645 can include an open model compiler socket 647 that can couple with a cell data plug-in(s) 649. The open model compiler 645 may use a set of cell data [[655]] 649 of interest.